REMARKS

By this amendment, claim 1 has been amended and claims 1-14 are active. This amendment is filed in reply to the outstanding Office Action of June 14, 2004, no new matter has been added and is believed to be fully responsive thereto and reconsideration is respectfully requested.

Specification and Claim Objection

The Examiner objected to the specification under 37 CFR 1.71 because it lacks an enabling description for claims 1-11, in reference to limitation "clock isolation elements" for logic and memory circuits, recited in claim 1. Further, the Examiner objected to claims 1-11 because of a typo error. In claim 1, line 7, the term "by pass" should be changed to "bypass."

Claim 1 has been amended to point out that the voltage isolation elements have independent clocking paths to each logic and memory macro circuits. This is more fully explained in the specification in paragraphs [24] – [27]. In addition, claim 1 has been amended to correct the typo error pointed out by the Examiner.

Rejection – 35 U.S.C. § 112

The Examiner rejected claims 1-11 under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The Examiner pointed out that claim 1, on line 8, recites "whereby ..." and concluded that such recitation is non-functional language, which is not given patentable weight.

The Applicants have amended claim 1 to remove the "whereby" and inserted structural cooperative relationships of the elements that explain the operation of BIST, while performing parallel tests of logic and memory elements.

Based on the foregoing, it is respectfully submitted that the claims are allowable under 35 U.S.C. § 112 second paragraph.

The Examiner rejected claims 1-11 under 35 U.S.C. § 112, first paragraph, as failing to comply with the enablement requirement. The Examiner indicated that the specification fails to describe the claimed limitation "clocking isolation elements" for logic and memory circuits, recited in claim 1.

As indicated above, the Applicants believe that the specification explains "clocking isolation elements" at paragraphs [24] - [27], as well as several other alternatives in preceding paragraphs and paragraphs following these paragraphs.

Applicants submit that adequate description is contained to support claims 1-11, which should be allowable under 35 U.S.C. § 112.

Rejection – 35 U.S.C. § 103

The Examiner rejected claims 1-14 under 35 U.S.C. § 103(a) as being unpatentable in view of Kraus et al. (US6587979).

The Applicants respectfully submit that Kraus et al. discloses nothing about parallel test of logic and memory. Kraus et al. indicates that logic is being tested by inference, and that logic is required to form the BIST engine to test the memory. The interpretation of the core wrapper as the "clocking isolation elements" is incorrect, as Kraus is using scan to set up the BIST and to read out data after the BIST has run and

then stopped and is not permitting scan to occur simultaneously with BIST. However, the present invention permits the scan to occur simultaneously, which is the key element of present invention.

Accordingly, it is respectfully submitted that claims 1-14 should be allowable under 35 U.S.C. § 103.

Conclusion

Based on the foregoing, it is respectfully submitted that all the claims active in the subject patent application are in condition for allowance and that the application may be passed to issuance.

The Examiner is urged to call the undersigned at the number listed below if, in the Examiner's opinion, such a phone conference would aid in furthering the prosecution of this application.

Respectfully submitted,

Robert A. Walsh

By: Robert A. Walsh, Reg. #26,516
IBM Intellectual Property Law 972E
1000 River Street
Essex Junction VT, 05452
(802) 769-9521/ fax: (802)769-8938

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